CLAIMS

What is claimed is:

1. A low noise amplifier having a substantially constant input impedance in an on mode as in an off mode, the low noise amplifier comprises:

input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive an input radio frequency (RF) signal;

an inductor having a first node and a second node, wherein the first node of the inductor is operably coupled to a power supply and the second node of the inductor is operably coupled to the drain of the input transistor to provide an output of the low noise amplifier; and

current sink having a first node and a second node, wherein the first node of the current sink is operably coupled to the source of the input transistor and the second node of the current sink is operably coupled to a circuit ground, wherein a real component of input impedance of the low noise amplifier is substantially constant when the low noise amplifier is in the off mode as when the low noise amplifier is in the on mode.

2. The low noise amplifier of claim 1 further comprises:

a variable capacitor circuit operably coupled to the gate of the input transistor, wherein the variable capacitor circuit provides a first capacitance value based on a first impedance selection signal when the low noise amplifier is in the off mode and provides a second capacitance value based on a second impedance selection signal when the low noise amplifier is in the on mode such that an imaginary component of the input impedance of the low noise amplifier is substantially constant when the low noise amplifier is in the off mode as when the low noise amplifier is in the on mode.

3. The low noise amplifier of claim 1, wherein the operable coupling between the second node of the inductor and the drain of the input transistor comprises:

a cascode transistor having a gate, a drain, and a source, wherein the source of the cascode transistor is operably coupled to the drain of the input transistor, the drain of the cascode transistor is operably coupled to the second node of the inductor, and the gate of the cascode transistor is operably coupled to receive a bias voltage.

4. The low noise amplifier of claim 1 further comprises:

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive one leg of the input RF signal and the gate of the input transistor is operably coupled to receive another leg of the input RF signal, and wherein the source of the second input transistor is operably coupled to the first node of the current sink; and

a second inductor having a first node and a second node, wherein the first node of the second inductor is operably coupled to the power supply and the second node of the inductor is operably coupled to the drain of the second input transistor to provide one leg of the output of the low noise amplifier.

5. The low noise amplifier of claim 4 further comprises:

each of the input transistor and the second input transistor having a width of W and a length of L, wherein parasitic capacitance of the input transistor and of the second input transistor is based on W; and

the current sink including a current mirror circuit and a current sink transistor operably coupled to the current mirror circuit, wherein the current sink transistor has a width of approximately 2W and a length of approximately 2L.

6. The low noise amplifier of claim 1 further comprises:

input capacitor operably coupled to provide the input RF signal to the gate of the input transistor.

7. The low noise amplifier of claim 1, wherein the operable coupling between the second node of the inductor and the drain of the input transistor comprises:

a cascode transistor having a gate, a drain, and a source, wherein the source of the cascode transistor is operably coupled to the drain of the input transistor, the drain of the cascode transistor is operably coupled to the second node of the inductor, and the gate of the cascode transistor is operably coupled to receive a bias voltage;

a first plurality of transistors, wherein each of the first plurality of transistors includes a gate, a drain, and a source, wherein the sources of each of the first plurality of transistors is operably coupled to the source of the cascode transistor and the drain of each of the first plurality of transistors is operably coupled to the drain of the cascode transistor, and wherein the gate of each of the first plurality of transistors is operably coupled to a corresponding one of a plurality of control signals; and

a second plurality of transistors, wherein each of the second plurality of transistors includes a gate, a drain, and a source, wherein the sources of each of the second plurality of transistors is operably coupled to the source of the cascode transistor and the drain of each of the second plurality of transistors is operably coupled to the power supply, and wherein the gate of each of the second plurality of transistors is operably coupled to a corresponding complementary one of the plurality of control signals.

8. A radio frequency integrated circuit (RFIC) comprises:

a transformer having a first winding and a second winding, wherein the first winding is operably coupled to an antenna for transceiving radio frequency (RF) signals;

baseband processing module operably coupled to convert outbound data into outbound baseband signals and to convert inbound baseband signals into inbound data based on a wireless communication protocol;

up conversion module operably coupled to convert the outbound signals into outbound RF signals;

a power amplifier operably coupled to the second winding of the transformer to transmit the outbound RF signals via the antenna;

a low noise amplifier operably coupled to the second winding of the transformer to receive inbound RF signals from the antenna; and

down conversion module operably coupled to covert the receive inbound RF signals into the inbound baseband signals, wherein the low noise amplifier includes:

input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive an input radio frequency (RF) signal;

an inductor having a first node and a second node, wherein the first node of the inductor is operably coupled to a power supply and the second node of the inductor is operably coupled to the drain of the input transistor to provide an output of the low noise amplifier; and

current sink having a first node and a second node, wherein the first node of the current sink is operably coupled to the source of the input transistor and the

second node of the current sink is operably coupled to a circuit ground, wherein a real component of input impedance of the low noise amplifier is substantially constant when the low noise amplifier is in the off mode as when the low noise amplifier is in the on mode.

9. The RFIC of claim 8, wherein the low noise amplifier further comprises:

a variable capacitor circuit operably coupled to the gate of the input transistor, wherein the variable capacitor circuit provides a first capacitance value based on a first impedance selection signal when the low noise amplifier is in the off mode and provides a second capacitance value based on a second impedance selection signal when the low noise amplifier is in the on mode such that an imaginary component of the input impedance of the low noise amplifier is substantially constant when the low noise amplifier is in the off mode as when the low noise amplifier is in the on mode.

10. The RFIC of claim 8, wherein the operable coupling between the second node of the inductor and the drain of the input transistor comprises:

a cascode transistor having a gate, a drain, and a source, wherein the source of the cascode transistor is operably coupled to the drain of the input transistor, the drain of the cascode transistor is operably coupled to the second node of the inductor, and the gate of the cascode transistor is operably coupled to receive a bias voltage.

11. The RFIC of claim 8, wherein the low noise amplifier further comprises:

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive one leg of the input RF signal and the gate of the input transistor is operably coupled to receive another leg of the input RF signal, and wherein the source of the second input transistor is operably coupled to the first node of the current sink; and

a second inductor having a first node and a second node, wherein the first node of the second inductor is operably coupled to the power supply and the second node of the inductor is operably coupled to the drain of the second input transistor to provide one leg of the output of the low noise amplifier.

12. The RFIC of claim 11, wherein the low noise amplifier further comprises:

each of the input transistor and the second input transistor having a width of W and a length of L, wherein parasitic capacitance of the input transistor and of the second input transistor is based on W; and

the current sink including a current mirror circuit and a current sink transistor operably coupled to the current mirror circuit, wherein the current sink transistor has a width of approximately 2W and a length of approximately 2L.

13. The RFIC of claim 8, wherein the low noise amplifier further comprises:

input capacitor operably coupled to provide the input RF signal to the gate of the input transistor.

14. The RFIC of claim 8, wherein the operable coupling between the second node of the inductor and the drain of the input transistor comprises:

a cascode transistor having a gate, a drain, and a source, wherein the source of the cascode transistor is operably coupled to the drain of the input transistor, the drain of the cascode transistor is operably coupled to the second node of the inductor, and the gate of the cascode transistor is operably coupled to receive a bias voltage;

a first plurality of transistors, wherein each of the first plurality of transistors includes a gate, a drain, and a source, wherein the sources of each of the first plurality of transistors is operably coupled to the source of the cascode transistor and the drain of each of the

first plurality of transistors is operably coupled to the drain of the cascode transistor, and wherein the gate of each of the first plurality of transistors is operably coupled to a corresponding one of a plurality of control signals; and

a second plurality of transistors, wherein each of the second plurality of transistors includes a gate, a drain, and a source, wherein the sources of each of the second plurality of transistors is operably coupled to the source of the cascode transistor and the drain of each of the second plurality of transistors is operably coupled to the power supply, and wherein the gate of each of the second plurality of transistors is operably coupled to a corresponding complementary one of the plurality of control signals.